IC WORKS

FEATURES

- **Provides 1x CPU, 2x CPU and 14.318MHz outputs**
- **Small 14 pin SOIC/DIP package**
- **Supports 3.3V and 5.0V operation**
- **Smooth, glitch-free frequency transistion**
- **TTL or CMOS input level compatible**
- **Integral loop filter components**
- **Advanced PLL design with low phase jitter**
- **High performance, low power CMOS**

FUNCTIONAL DESCRIPTION

The W42C25 is a solution for generating three simultaneous clocks while using minimum board space. One clock (REFCLK) is a fixed output frequency which is the same as the input reference crystal (or clock). The other clocks (CPUCLK and 2xCPUCLK) can vary between 2 and 120MHz with up to 8 selectable programmed frequencies stored in internal ROM.

Included in the W42C25's advanced features are three-state outputs and on-chip loop filters. Jitter free operation is provided with only two decoupling capacitors. Smooth and glitch-free transitions are offered when switching from one frequency to another. This feature can be utilized in power management systems such as notebooks and palmtop computers where it is frequently necessary to slow down the clock to preserve power. This device is designed to be compatible with the Intel cycle to cycle timing specifications for the 80486 processors.

Custom masked versions, with customized frequencies are available upon request.

FUNCTIONAL BLOCK DIAGRAM: W42C25
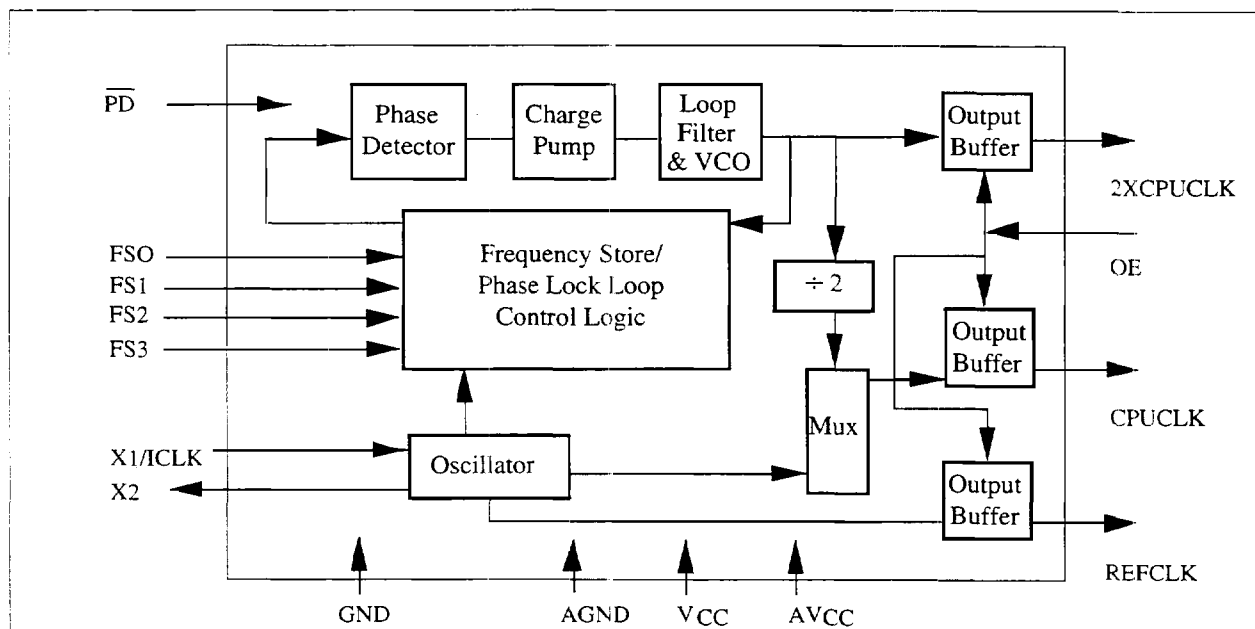
PIN DESCRIPTIONS: W42C25

Pin Name	Input/Output	Function
2XCPUCLK	O	Clock Output (refer to Frequency Selection Table)
AGND	-	Analog ground connection
AV$_{CC}$	-	Analog power supply connection
CPUCLK	O	Clock Output (refer to Frequency Selection Table)
FS0	I	Frequency Selection input, LSB (Note 1)
FS1	I	Frequency Selection input (Note 1)
FS2	I	Frequency Selection input, MSB (Note 1)
GND	-	Ground connection
OE	I	Output Enable, puts all outputs in high impedance state when low (Note 1)
REFCLK	O	Reference Clock output, outputs crystal or input clock frequency
$\overline{\text{SLOWCPU}}$	I	Slow CPU input. Slows 2XCPUCLK output to 16MHz and CPUCLK output to 8MHz when low (Note 1)
$\overline{\text{PD}}$	I	Power Down input, puts W42C08 in power down mode when low (Note1)
V$_{CC}$	-	Power supply connection
X1/ICLK	I	Crystal connection or external clock frequency input
X2	O	Crystal connection, leave unconnected when using external clock

Note 1: All inputs, except for X1/ICLK, have an internal pull-up resistor. Unconnected inputs will assume a logic high condition.

PIN CONFIGURATIONS: W42C25

W42C25-02
Top View

```
      FS1 ⊏ 1  U 14 ⊐ FSO
      FS2 ⊏ 2    13 ⊐ CPUCLK
   REFCLK ⊏ 3    12 ⊐ AVCC
     AGND ⊏ 4    11 ⊐ VCC
      GND ⊏ 5    10 ⊐ 2XCPUCLK
       PD ⊏ 6     9 ⊐ OE
  X1/ICLK ⊏ 7     8 ⊐ X2
```

W42C25-07
Top View

```
      FS1 ⊏ 1  U 14 ⊐ FSO
      FS2 ⊏ 2    13 ⊐ CPUCLK
   REFCLK ⊏ 3    12 ⊐ AVCC
     AGND ⊏ 4    11 ⊐ VCC
      GND ⊏ 5    10 ⊐ 2XCPUCLK
  SLOWCPU ⊏ 6     9 ⊐ OE
  X1/ICLK ⊏ 7     8 ⊐ X2
```

FREQUENCY SELECTION FOR W42C25-02, -07 (using 14.318MHz input)

FS2, FS1, FS0	2XCPUCLK (MHz)	CPUCLK (MHz)	REFCLK (MHz)
000	25	12.5	14.318
001	33.3	16.6	14.318
010	40	20	14.318
011	50	25	14.318
100	60	30	14.318
101	66.6	33.3	14.318
110	80	40	14.318
111	100 (Note 2)	50 (Note 2)	14.318

Note 2: Not guaranteed when Vcc < 4.5V.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}, V_{IN}	-0.5 to 7.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Ambient Temperature Under Bias	T_B	-55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

Note 1: Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AT 5.0V
DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5 V \pm 10$ %)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2		10	20	mA
Input Low Voltage	V_{IL}	$V_{CC} = 5V$			0.8	V
Input High Voltage	V_{IH}	$V_{CC} = 5V$	2.0			V
Output Low Voltage	V_{OL}	$I_{OL} = 8 mA$			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4 mA$	2.4			V
Output Freq. Change	F_D	Over supply and temperature		.002	.01	%
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Input Low Current	I_{IL}	$V_{IN} = 0V$ (incls pull-up resistor)			-100	µA
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			10	µA
Standby Supply Current	I_{STDBY}	$V_{CC} = 5.0V$ PD = 0V		25		µA
Input Pull-Up Resistor	R_P	$V_{IN} = 0V$		250		kΩ

Note 2: W42C25-02 with no load, with 14.318 MHz crystal input, and CPUCLK running at 40 MHz. Power supply current varies with frequency.

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10$ %)

Parameter	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_W	20			ns
Setup Time Data to Enable	T_{SU}	20			ns
Output Frequency	F_O	2		120	MHz
Input Frequency	F_I	2	14.318	32	MHz
Hold Time Data to Enable	T_{HD}	10			ns
Input Clock Rise Time	$ICLK_r$			20	ns
Input Clock Fall Time	$ICLK_f$			20	ns
Output Rise Time, 0.8 to 2.0V, 25pF Load	T_R		1	2	ns
Rise Time, 20 to 80% V_{CC}, 25pF Load	T_R		2	4	ns
Output Fall Time, 2.0 to 0.8V, 25pF Load	T_F		1	2	ns
Fall Time, 80 to 20% V_{CC}, 25pF Load	T_F		2	4	ns
Duty Cycle, 15pF Load	D_T	40	50/50	60	%
Jitter, 1 Sigma, All Frequencies	T_{J1S}		±0.5	±2	%
Jitter, Absolute, All Frequencies	T_{JABS}		±3	±5	%
Frequency Transition Time, 50 to 4MHz	T_{FT}			20	ms
Powerup Time, Off to 100MHz	T_{PU}		15	30	ms
Clock Skew; CPUCLK vs 2XCPUCLK	T_{SK}		±0.5	±1.0	ns

ELECTRICAL CHARACTERISTICS AT 3.3V

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 3.3V \pm 10\%$) (Note 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2		8	16	mA
Input Low Voltage	V_{IL}	$V_{CC} = 3.3V$			0.15Vcc	V
Input High Voltage	V_{IH}	$V_{CC} = 3.3V$	0.7Vcc			V
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
Output Freq. Change	F_D	Over supply and temperature		.002	.01	%
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		20		pF
Input Low Current	I_{IL}	$V_{IN} = 0V$ (incl. pull-up res.)			-100	μA
Input High current	I_{IH}	$V_{IN} = V_{CC}$			10	μA
Standby Supply Current	I_{STDBY}	$V_{CC} = 3.3V$ PD = 0V		25		μA
Input Pull-Up Resistor	R_P	$V_{IN} = 0V$		250		kΩ

Note 2: lu42C08-03 with no load, with 14.318 MHz crystal input, and CLK1 running at 40 MHz. Power supply current varies with frequency and output load capacitance.

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameter	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_W	20			ns
Setup Time Data to Enable	T_{SU}	20			ns
Output Frequency (CPUCLK & 2XCPUCLK)	F_O	2		80	MHz
Input Frequency	F_I	2	14.318	32	MHz
Hold Time Data to Enable	T_{HD}	10			ns
Input Clock Rise Time	$ICLK_R$			20	ns
Input Clock Fall Time	$ICLK_F$			20	ns
Rise Time, 20 to 80% V_{CC}, 15pF load	T_R		2	4	ns
Fall Time, 80 to 20% V_{CC}, 15pF Load	T_F		2	4	ns
Duty Cycle, 15pF Load	D_T	40	50/50	60	%
Jitter, 1 Sigma, All Frequencies	T_{J1S}		±0.5	±2	%
Jitter, Absolute, All Frequencies	T_{JABS}		±3	±5	%
Frequency Transition Time, 50 to 4MHz	T_{FT}			20	ms
Powerup Time, Off to 100MHz	T_{PU}		15	30	ms
Clock Skew; CPUCLK vs 2XCPUCLK	T_{SK}		±0.5	±1.0	ns

RECOMMENDED CIRCUIT CONFIGURATION
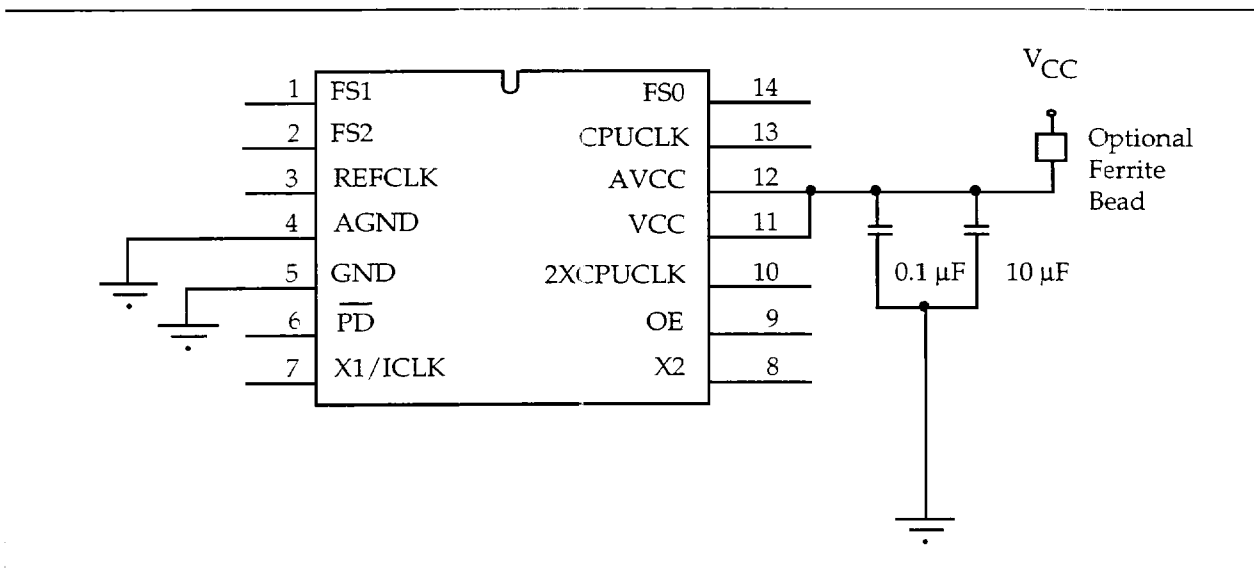
RECOMMENDED BOARD LAYOUT: ⴜ42C25

For optimum performance in system applications, the above power supply decoupling scheme should be used. Both GND pins are connected directly to the power plane.
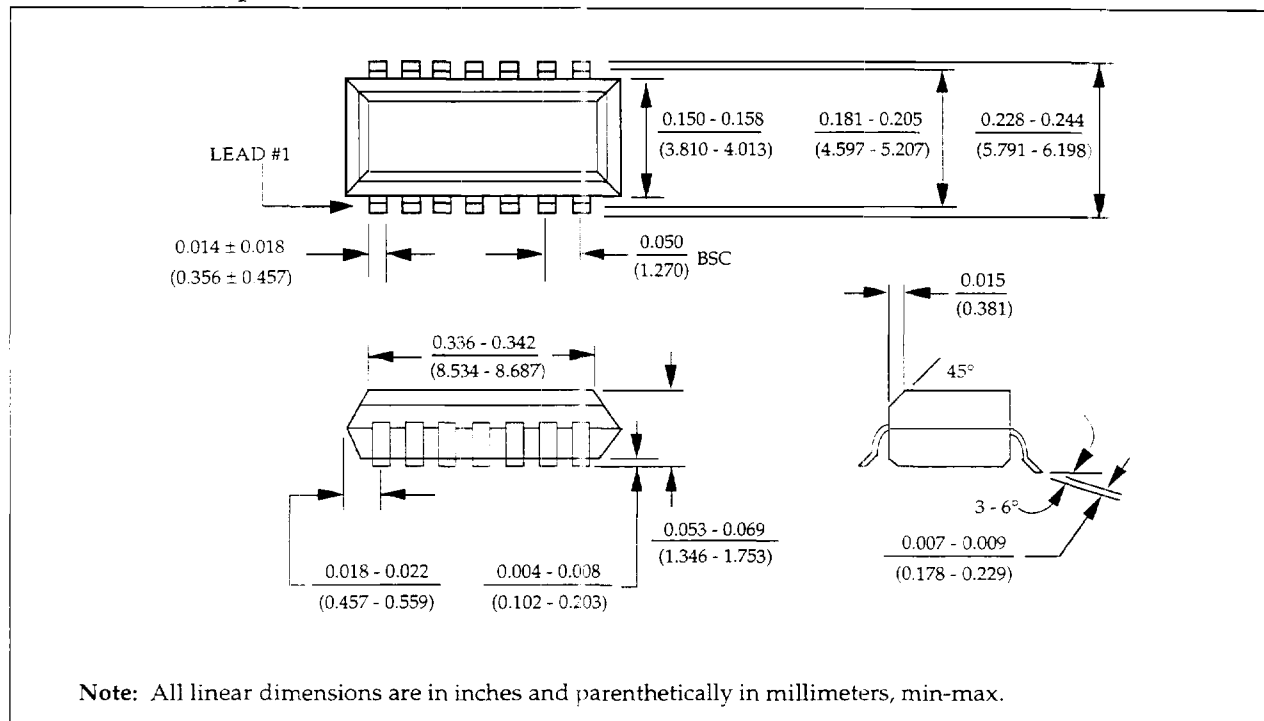
VCC decoupling is important to reduce phase jitter and EMI radiation. The 0.1μF decoupling capacitor should be placed as close to its VCC pins as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10μF decoupling capacitor shown is optional but will improve power supply rejection. It should be a tantalum type. For further EMI protection, the VCC connection can be made via a ferrite bead, as shown above.

An isolated ground plane should *not* be used, even though this is a common recommendation. An isolated ground plane works well when the clock source and load share the same isolated ground area, however, this is not the case with a CPU motherboard. Ground plane isolation will only cause increased EMI, ground bounce, and in many cases increased output clock jitter.
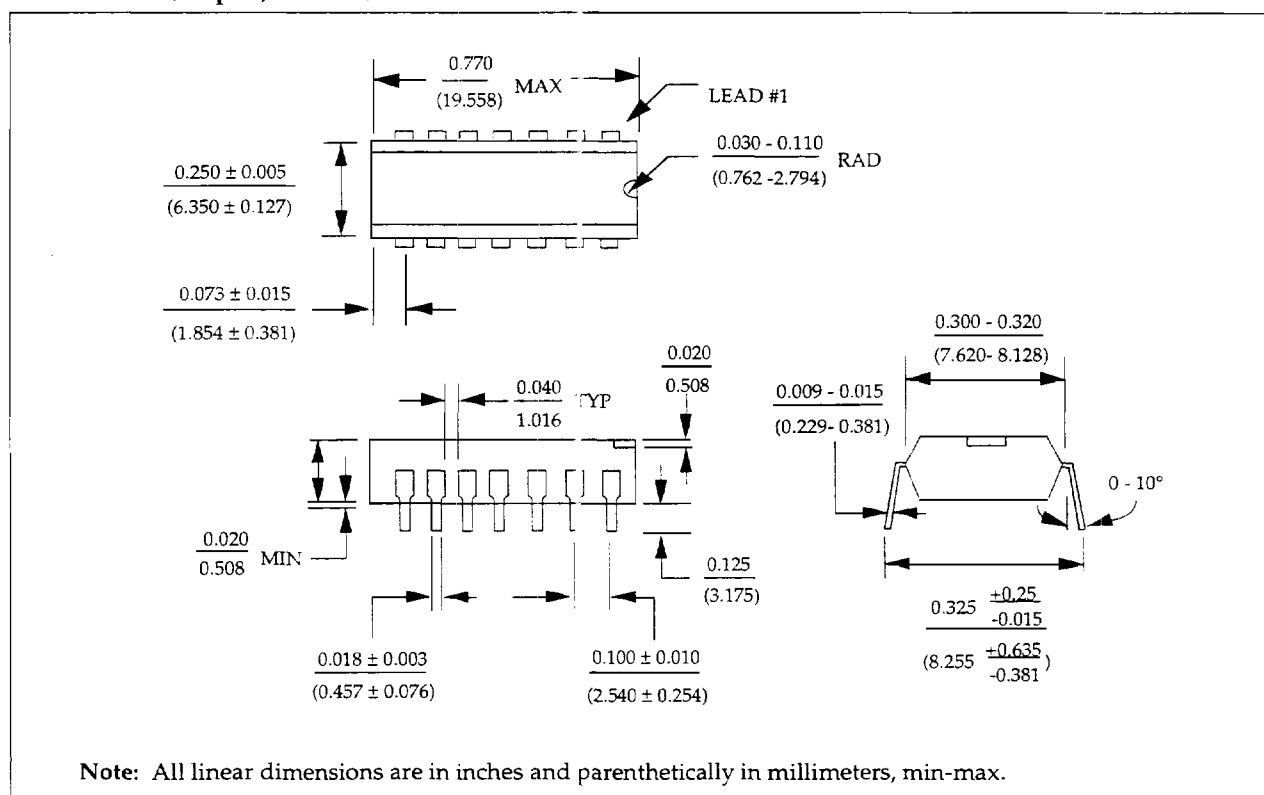
When using the ⴜ42C25, unused input select pins may be tied to either ground or VCC, or may be left unconnected; since internal pull-up resistors are incorporated on all logic input pins, an unconnected input will assume a logic 1 condition. Output clocks should use a series tremination resistor (about 33 ohms) placed as close to the clock outputs as possible; this will also help to decrease jitter and EMI.
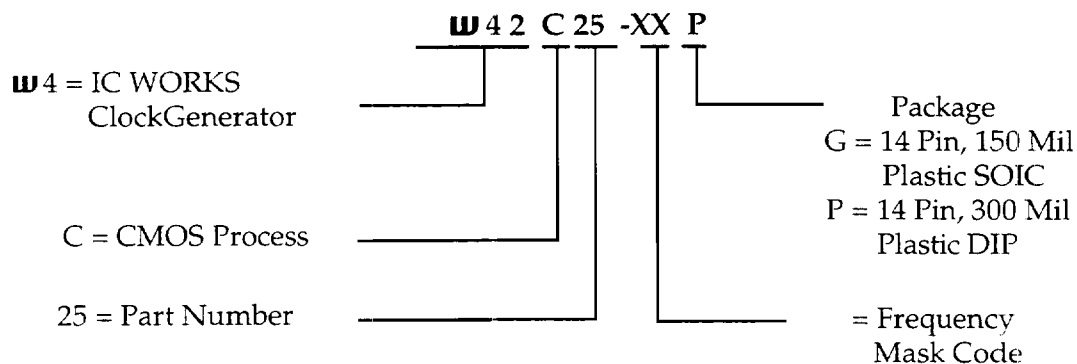
PACKAGING INFORMATION

Plastic SOIC (14 pin, 150mil)

LEAD #1

0.150 - 0.158 (3.810 - 4.013)

0.181 - 0.205 (4.597 - 5.207)

0.228 - 0.244 (5.791 - 6.198)

0.014 ± 0.018 (0.356 ± 0.457)

0.050 (1.270) BSC

0.015 (0.381)

45°

0.336 - 0.342 (8.534 - 8.687)

0.053 - 0.069 (1.346 - 1.753)

3 - 6°

0.007 - 0.009 (0.178 - 0.229)

0.018 - 0.022 (0.457 - 0.559)

0.004 - 0.008 (0.102 - 0.203)

Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

Plastic DIP (14 pin, 300mil)

0.770 (19.558) MAX

LEAD #1

0.030 - 0.110 (0.762 - 2.794) RAD

0.250 ± 0.005 (6.350 ± 0.127)

0.073 ± 0.015 (1.854 ± 0.381)

0.040 1.016 TYP

0.020 0.508

0.009 - 0.015 (0.229 - 0.381)

0.300 - 0.320 (7.620 - 8.128)

0 - 10°

0.020 0.508 MIN

0.125 (3.175)

0.325 +0.25 / -0.015

(8.255 +0.635 / -0.381)

0.018 ± 0.003 (0.457 ± 0.076)

0.100 ± 0.010 (2.540 ± 0.254)

Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

ORDERING INFORMATION

W 4 2 C 25 -XX P

W4 = IC WORKS
      ClockGenerator

C = CMOS Process

25 = Part Number

Package
G = 14 Pin, 150 Mil
      Plastic SOIC
P = 14 Pin, 300 Mil
      Plastic DIP

= Frequency
  Mask Code

VALID PART NUMBERS

W42C25-02G   W42C25-07G
W42C25-02P   W42C25-07P

IC WORKS

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